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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,923	04/16/2001	Shigeo Onishi	925-190	5436

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EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,923	ONISHI, SHIGEO	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The non-final rejection as set forth in paper No.10 is withdrawn in response to applicants' amendments.

2. A new rejection is made as set forth in this Office Action.

3. Claims 1-7 and 9-12 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda et al. (U.S. 6,335,241 B1) in view of Zurcher et al. (U.S. 6,344,413 B1).

In reference to claims 1-6, Hieda et al. (Figs.1-5 and 18-23) in a related method to form a stacked DRAM capacitor teach the steps of sequentially forming an interlayer insulating film (14) and a barrier film (15/21) comprising silicon nitride on a semiconductor substrate (1); making a contact hole in the barrier film (15/21) and the interlayer insulating film (14) and forming a plug (20) within the contact hole; forming an insulation film (22) on the plug (20) and the barrier film (15/21) and then forming a hole in the insulation film (22) leading to the plug (20) such that an upper surface of the plug (20) and part of the barrier film is exposed; forming a first conductive film in the insulation film (22) and on and over an exposed part of the barrier film (15/21) in the hole such that the hole in the insulation film (22) is filled with the first conductive film,

and then etching the first conductive film by a chemical mechanical polishing to thereby form a lower electrode (24) within the hole in the insulation film; etching the insulation film (22) until the barrier film (15/21) is exposed, so as to leave the lower electrode (24) in a protuberant manner; forming a dielectric film (26) that covers the protuberant lower electrode (24) and at least part of the barrier film (15/21), and then forming a second conductive film (27) that covers the dielectric film (26), said dielectric film (26) being made of a ferroelectric or high-dielectric-constant substance (column 10, line 5 – column 16, line 7).Also in another embodiment of the invention, Hieda et al. (Fig.30D) teach patterning the dielectric layer and the second conductive film to thereby form a capacitor dielectric film and an upper electrode (column 21, lines 37 – 42).

Furthermore, in reference to claim 4, Hieda et al. in another embodiment of the invention (Figs.24-25) teach forming a cup-shaped capacitor including the steps of forming a first conductive film over at least part of the first insulation film and within the hole such that the first conductive film within the hole does not fill the hole but covers the surfaces defining the hole, and then forming a second insulation film on the first conductive film; and then etching the first conductive film and the second insulation film in the hole by a chemical mechanical polishing method until the first insulation film is exposed, to thereby form a cup-shaped lower electrode within the hole; and etching the first insulation film and the second insulation film within the hole until the barrier film (15/21) and the lower electrode (24) are exposed (column 16, line 63 – column 17, line 47).

However, Hieda et al. fail to teach forming an insulation film and an adhesion film on the plug and the barrier film, and then forming a hole in the insulation film and the adhesion film leading to the plug such that an upper surface of the plug and an adjacent part of the barrier film are exposed; wherein said adhesion film comprises titanium and wherein the adhesion film is removed before the lower electrode is left in the protuberant manner. Also, Hieda et al. fail to expressly teach forming a second insulation film on the first conductive film so as to fill the hole; and etching the second insulation film until an upper surface of the first conductive film is reached.

Nevertheless, Zurcher et al. (Figs.11-16) in a related method to form a DRAM device teach depositing an insulation film (206, 218) over a barrier film (207); forming a hole on the insulation film, thereby exposing an upper surface of a plug (204) and an adjacent part of the barrier film (207); forming a conductive layer (208, 210) on the insulation film (206, 218) and exposed areas of the barrier film (207) and the upper surface of the plug (204), wherein an adhesion film comprising titanium is deposited between the insulation film (206, 218) and the conductive film (208, 210) to improve adhesion between both layers; and performing a planarization process, exposing the insulation film (206, 218) (column 6, lines 28 – 43). Also, Zurcher et al. teach forming a second insulation film (240) on the first conductive film (208, 210) so as to fill the hole; and etching the second insulation film (240) until an upper surface of the first conductive film (208, 210) is reached (column 6,lines 43 – 68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made include forming an adhesion layer of Zurcher et al. after

forming the insulation film of Hieda et al., thus removing the adhesion film and the insulation film before the lower electrode is left in the protuberant manner, since this would improve the adhesion of the conductive layer to the insulation film (Zurcher et al., column 6, lines 28 – 43). Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zurcher et al. and Hieda et al. to enable forming the a hole on the insulation film so that portions of the barrier film and the upper surface of the contact plug are exposed. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zurcher et al. and Hieda et al. to enable forming a second insulation film on the first conductive film so as to fill the hole, and etching the second insulation film until an upper surface of the first conductive film is reached as taught by Zurcher et al.

In reference to claims 7 and 9, Hieda et al. teach the second conductive film is formed such that a gap defined between opposite surfaces of the dielectric film within the hole is filled with a part of the second conductive film (see Fig.25B); and a part of the upper electrode fills a gap defined between opposite surfaces of the dielectric film within the hole (see Fig.25B).

In reference to claims 10-12, Hieda et al. teach a contact hole having the same cross sectional area in both the interlayer insulating film and the barrier film; and the dielectric film (57) covering each of an upper surface and all side surfaces of the protuberant lower electrode (60) (Fig.30B).

Response to Arguments

6. Applicant's arguments with respect to claims 1-7 and 9-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
7/16/03

George Fourson
Primary Examiner